Project profile

CT302 | Towards one European test solution (TOETS)

PROJECT CONTRIBUTES TO

Communication	✔
Automotive and transport	✔
Health and aging society	✔
Safety and security	
Energy efficiency	✔
Digital lifestyle	
Design technology	✔
Sensors and actuators	
Process development	
Manufacturing science	✔
More than Moore	✔
More Moore	
Technology node	45/40 & 32/28 nm

MANUFACTURING SCIENCE

Partners:
ADD
ATMEL
CEA-LETI
CEA-LIST
D4T Systems
e2v semiconductors
IMSE-CNM
INESC Porto
Infineon
iRoC
JTAG
KU Leuven
LIRMM
NXP Semiconductors
Optimalia SAS
Q-Star Test
Salland Engiineering
STMicroelectronics
SUPELEC
Temento
Tomorrow Options Microelectronics
TIMA
Uni Twente

Project leader:
Kees Veelenturf
NXP Semiconductors

Key project dates:
Start: March 2009
End: March 2012

Countries involved:
Austria
Belgium
France
The Netherlands
Portugal
Spain

Testing takes an increasingly significant proportion of total production costs for advanced semiconductor devices as miniaturisation and integration levels rise. For system-on-chip and system-in-package designs, such testing can be up to 20% of the total cost of chip design and manufacture – and this is increasing drastically as complexity and functionality grow. Yet often, 80 to 90% of this testing concentrates on the analogue, mixed analogue-digital signal and embedded radio-frequency parts of the design. The TOETS project focuses on developing new methods to bring down the cost of such testing, and is addressing the challenge at application, chip architecture and transistor technology levels.

The coming decade will introduce advances in electronic applications that will change the way we live. Advanced personal healthcare, improved on-the-road safety and secured communications are just a few examples. Such applications will be based on highly integrated nanotechnology semiconductor design, where reliability and trustworthiness will be critical factors.

This reliability depends upon extensive – and hence costly – testing throughout the lifetime of the product. If this testing process could be built into the design, it would have a radical effect on chip design, manufacture and operation costs. This is the focus of the CATRENE CT302 TOETS project.

TOETS involves five large companies, nine small and medium-sized enterprises (SMEs) and eight universities and research institutes across Europe. The project aims to create a real breakthrough in semiconductor design methods and flows by considering the test function throughout the value chain, from silicon to application.

Road to self-repairing chip

Although important advances have been made recently, existing test solutions are still unable to cover exhaustively all types of defects occuring in new technologies, and often fail to deal with the yield loss resulting from manufacturing process variations. This trend will be exacerbated in the future with the emergence of new technology nodes – 45 nm, 32 nm and beyond – and the integration of various technologies such as digital, analogue, memory and radio frequency (RF) into a single system, be it system-on-chip (SoC) or system-in-package (SiP).

Testing is a major contributor to the manufacturing costs of a product. Digital test methods such as scan test, scan-compression techniques, built-in self test (BIST) and boundary scan – IEEE 1149.1 – have been widely adopted in the industry. The penetration of these test provisions in SoC devices for example is typically greater than 90%. These test provisions, which were a main working area in the MEDEA+ NanoTEST project have reduced the test share of total costs for the digital parts of a SoC device to typically 10 to 20%.

However, 80 to 90% of SoC test costs are spent on checking analogue, mixed-signal and embedded RF blocks. This is mainly due to the long test-times caused by specification-based testing, as well as the expense of instrumentation, which brings little opportunity for multi-site testing.

TOETS will focus on reducing the test costs for analogue, mixed-signal and RF testing by providing new design-for-test (DfT) and BIST solutions to bring down the test-cost proportion of manufacturing SoC designs. The CATRENE project is structured around three work packages, which address the technical challenges at the application, chip archi-

tecture and transistor technology levels. These three work packages are the first steps along the road to the ultimate goal of autonomous self-adjustable and self-repairable chips.

Making this vision a reality requires insight at the technology level to know what can go wrong, and internal test solutions to detect and correct/repair these anomalies within an application while it is in normal operation. In this context, testing is no longer just a cost factor, but an added-value feature to be made use of by the end-integrator and end-user.

Introducing novel test methods

The project has two key objectives, to:

1. Improve quality levels by introducing novel test methods. In the automotive sector for example, the safety integrity level (SIL) is typically specified on a one-to-four scale. A SIL4 level means that the probability of a fault occurrence per hour must be lower than 10^{-9}. With the increasing number and complexity of embedded systems, meeting such a goal is increasingly challenging. TOETS will contribute to reaching such a target not only by improving quality at the chip design and manufacturing levels, but also by providing test, diagnosis and repair functions within the final application; and
2. Reduce test-development lead times and costs. TOETS hopes to improve the so-called CoT/CoS ratio – relating the cost of testing to the overall cost of chip development and production. The CATRENE project intends to prove a productivity gain in testing that surpasses those in wafer production and assembly. Typically, as miniaturisation and integration techniques advance, the CoT/CoS ratio would be expected to increase.

   However TOETS aims to stabilise CoT/CoS by pursuing an aggressive goal of surpassing the productivity gain of other domains and further improving the CoT/CoS ratio – by for example 10% – through innovations and breakthroughs. Furthermore, the project is targeting a reduction of 40% in test development lead-time.

Helping compete in global markets

Progress in microelectronics design and manufacturing is normally measured in terms of ever greater integration, a process which not only brings increasing complexity, but also new challenges in the form of process variability and types of defect. European industries have until now been able to retain their ability to face competition in this area, but only at the cost of a continuing effort to maintain this position.

The results of TOETS will support new business development in the domains of security, healthcare, transportation and communication, the automotive sector and industrial electronics. They will do so by reducing test costs for new packages such as SiP designs, SoC developments with embedded RF and mixed-signal interfaces, and micro-electromechanical systems (MEMS) products.

TOETS will contribute significantly to the partners' ability to compete in world markets and, thus, to extend both business and employment. The project will safeguard high-qualification jobs within the European microelectronics industry, and will also create opportunities in the SME sector by providing access to the high-tech results of large companies, and offering the potential of new business relationships with the members of the consortium.

This CATRENE project also supports the European effort towards a leading global position in complete chip solutions that combine digital, analogue and RF blocks. This is a key goal in ensuring that chip designs can be manufactured at market-compliant cost. In the automotive industry, for example, future quality requirements are expected to be less than one part per million (ppm) with a target to reach zero ppm, while the manufacturing yield in advanced technologies is typically lower than 90% – equivalent to 100,000 ppm.

CATRENE Office
9 Avenue René Coty - F-75014 Paris - France
Tel.: +33 1 40 64 45 60 - Fax: +33 1 45 48 46 81
Email: catrene@catrene.org
http://www.catrene.org

CATRENE (Σ! 4140), the EUREKA **C**luster for **A**pplication and **T**echnology **R**esearch in **E**urope on **N**ano**E**lectronics, will bring about technological leadership for a competitive European information and communications technology industry.

CATRENE focuses on delivering nano-/microelectronic solutions that respond to the needs of society at large, improving the economic prosperity of Europe and reinforcing the ability of its industry to be at the forefront of the global competition.