Monday, January 23, 2017		Room 26
8:15 AM - 9:00 AM	HiPEAC Opening	Main Hall A1
8:45 AM - 10:00 AM	**HiPEAC Keynote**	Main Hall A1
10:00 AM - 10:15 AM	**Opening Session** by Christos Bouganis (Imperial College London, UK), Vanderlei Bonato (University of São Paulo), Juergen Becker (KIT, Germany), and João M.P. Cardoso (Univ. of Porto, Portugal)	
10:15 AM - 11:00 AM	***Invited Talk:*** ***QUANTUM COMPUTING FOR ENGINEERS*** *, by* ***Koen Bertels*** *and* ***Carmen Almudever*** *(TUDelft, The Netherlands)* *Chair: Juergen Becker, KIT, Germany*	
11:00 AM - 11:30 AM	*Coffee Break*	
11:30 AM - 12:45 PM	*EU Project Session:* ***The DeSyRe project: On-Demand Adaptive and Reconfigurable Fault-Tolerant SoCs*** *by* ***Ioannis Sourdis*** *(Chalmers University of Technology, Sweden)* ***An open tools platform for exploiting reconfigurability in HPC nodes*** *by* ***Dirk Stroobandt*** *(Univ. of Ghent, Belgium)* ***The SiLago Method: Next Generation VLSI Architecture and Design Methods*** *by* ***Ahmed Hemani*** *(KTH – Royal Institute of Technology, Kista, Sweden)* *Chair : João M.P. Cardoso, Univ. of Porto, Portugal*	
1:00 PM - 2:00 PM	*Lunch & Exhibition*	
Paper Session	Session A Chair: Dirk Stroobandt, Univ. of Ghent, Belgium	Authors
2:00 PM - 2:22 PM	*Title: High Level Synthesis versus HDL: A Case study on Hardware Accelerators for Financial Applications*	Ioannis Stamoulias, Christoforos Kachris and Dimitrios Soudris
2:22 PM - 2:44 PM	*Title:Code Compression Technique Based on Flexible Bin-Packing Algorithm*	Hochan Lee and Bernhard Egger
2:44 PM - 3:06 PM	*Title: Dynamic-pattern string matching SoC based on Boyer-Moore algorithm*	Adrian Dominguez
3:06 PM - 3:28 PM	*Title: A Decoupled Access-Execute Architecture for Reconfigurable Accelerators*	George Charitopoulos, Charalampos Vatsolakis, Stefanos Sidiropoulos, Grigorios Chrysos and Dionisios Pnevmatikatos
3:30 PM - 4:00 PM	*Coffee Break*	
4:00 PM - 4:50 PM	*Industrial Session:* ***Elastic Dataflow Computing for the Masses*** *by* ***Tobias Becker*** *(Maxeler Technologies, UK)* ***TBD, by Katerina Paulsson*** *(Ericsson AB, Sweden)* *Chair: Christos Bouganis, Imperial College London, UK*	
Paper Session (Short)	Session B Chair: Vanderlei Bonato, University of São Paulo, Brazil	Authors
4:50 PM - 5:00 PM	*Title: Towards the ultimate flexible fixed-point function generator for FPGAs*	Bogdan Pasca and Matei Istoan
5:00 PM - 5:10 PM	*Title: Improved Dynamic Cache Sharing for Communicating Threads on a Runtime-Adaptable Processor*	Joost Hoozemans, Arthur Lorenzon, Antonio Carlos Schneider Beck Filho and Stephan Wong
5:10 PM - 5:20 PM	*Title: On-Demand Selective Region Scrubbing in FPGAs with an LUT-grain Fault Masking and Detection*	Umar Afzaal and Jeong A Lee
5:20 PM - 5:30 PM	**Closing Session**	